Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.128”**

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**.128”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: B = .012” x .052”**

 **E = .012” x .084”**

**Backside Potential: COLLECTOR**

**APPROVED BY: DK DIE SIZE .128” X .128” DATE: 12/15/22**

**MFG: MICROSEMI THICKNESS .010” P/N: 2N6193**

**DG 10.1.2**

#### Rev B, 7/19/02